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Examiner: Michael Trinh

Group Art Unit: 2822 Docket: 303.324US2

S/N 09/256.643

IN THE UNITED STATES PATE TAND TRADEMARK OFFICE

APR 1 7 2000

Applicant:

Leonard Forbes et al.

Serial No.:

09/256,643

Filed:

February 23, 1999

Title:

TRANSISTOR WITH VAR AND ECTRON AFFINITY GATE AND

METHODS OF FABRICATION AND USE

## RESPONSE TO RESTRICTION REQUIREMENT AND PRELIMINARY AMENDMENT

Assistant Commissioner for Patents Washington, D.C. 20231

APR 2 0 2000

**TECHNOLOGY CENTER 2800** 

Prior to examination, please amend the above-identified application as follows:

## **ELECTION/RESTRICTION**

In response to the Restriction Requirement mailed March 14, 2000, Applicants elect, without traverse, Group I (claims 21-33). Applicants respectfully cancel remaining claims 34-35 without prejudice, and reserve the right to reintroduce them in a divisional application at a later date.

## IN THE CLAIMS

Please amend the following claims:

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21.(Amended) A method of [producing] <u>fabridating</u> a transistor [on] in a semiconductor substrate, the method comprising:

forming a source region and a drain [regions] region in a semiconductor substrate,

[thereby defining] a channel region being between the source region and the drain region

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01 FC:103 02 FC:102 36 60 filling an insulating layer on the channel region; and

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound Si<sub>1-r</sub>C<sub>r</sub>; and

selecting x at a predetermined value approximately between 0 and 1.0.

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29.(Amended) The method of claim 21, wherein [fabricating the gate includes the steps of] forming a gate further comprises:

depositing the silicon carbide compound  $Si_{1-x}C_x$  on the insulating layer using low pressure

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